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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO.
09.627,979	07.28.2000	Randy H. Y. Lo	UPA-00156	3057

7590 07.01.2003

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EXAMINER

NGUYEN, DILINH P

ART UNIT PAPER NUMBER

2814

DATE MAILED: 07.01.2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/627,979	LO ET AL.
Examiner	Art Unit	
DILINH NGUYEN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 12 June 2003.

2a) This action is FINAL.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 41-45, 47-54, 56 and 57 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 41-45, 47-54 and 56-57 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) Notice of References Cited (PTO-892)                            4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)                    5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_                    6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 41-45 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Pat. 6301121) and Akram et al. (U.S. Pat. 5994166) in view of Rostoker et al. (U.S. Pat. 5648661).

Lin discloses a multi-chip module package structure (fig. 1A, column 1, lines 33 et seq.) comprising:

a multi-chip module substrate;  
at least two chip packages, each of the chip packages being a packaged chip module having a bare chip a chip substrate packaged and enclosed therein;  
a plurality of electrical connect points electrically connecting the chip packages with the multi-chip module substrate; and

wherein the multi-chip module package structure is a ball grid array package (fig. 2A, column 4, line 29).

Lin fails to disclose the chip packages having been burn-in tested and function tested; a plurality of electrical connect pins; and a package material enclosing the multi-chip module substrate, the connect points and the chip packages.

Akram et al. disclose a semiconductor device (cover fig.) comprising:

a plurality of electrical connect pins 114 (column 5, line 64); a package material 172 (column 6, line 26) enclosing a multi-chip module substrate 102, a connect points 126 and a chip packages to achieve densely packaged semiconductor device (abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lin to achieve densely packaged semiconductor device, as shown by Akram et al.

Lin and Akram et al. fail to disclose the chip packages having been burn-in tested and function tested.

Rostoker et al. disclose a plurality of dice 102 have passed both burned- in and function tests (figs. 2A-3A, column 8, lines 45-58 and column 30, lines 31-37) to detect chips that are defective at wafer level and reduce the cost for the semiconductor device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lin and Akram et al. to detect chips that are defective at wafer level by burn in tested, function tested and reduce the cost for the semiconductor package device, as shown by Rostoker et al.

- Regarding claim 42, Lin discloses the chip package is a chip scale package (column 1, lines 33-34).
- Regarding claim 43, Lin discloses at least one of the chip packages is a chip scale package with wire bonding.
- Regarding claim 44, Akram et al. disclose a chip 162 is a chip scale package with flip chip bonding (column 6, lines 44-48).

- Regarding claim 45, it would have been obvious to one having ordinary skill in the art to form one of the chip packages is a central pad bonding package.
- Regarding claim 47, Akram et al. disclose the plurality of electrical connect pins are solder balls.
- Regarding claim 48, Lin discloses the plurality of electrical connect points are solder balls.

3. Claims 49-54 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka (U.S. Pat. 5784264) in view of Rostoker et al. (U.S. Pat. 5648661).

Tanioka discloses a multi-chip module package structure (fig. 1, column 1, lines 39 et seq.) comprising:

    a multichip module substrate 10 (column 1, line 41);  
    at least a bare chip 7;  
    at least one chip package being a packaged chip module having a bare chip 2 and a chip substrate packaged 11 and enclosed therein;  
    a plurality of electrical connect points electrically connecting the bare chip and at least one chip package with the multi chip module substrate;  
    a plurality of electrical connect pins 14;  
    a package material 16 enclosing the chip module substrate, the connect points, the bare chip and at least one chip package; and  
    wherein the multi-chip module package structure is a ball grid array package (column 4, lines 5-8).

Tanioka fails to disclose at least one chip package having been burn in tested and function tested.

Rostoker et al. disclose a plurality of dice 102 have passed both burned- in and function tests (figs. 2A-3A, column 8, lines 45-58 and column 30, lines 31-37) to detect chips that are defective at wafer level and reduce the cost for the semiconductor device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Tanioka to detect chips that are defective at wafer level by burn in tested, function tested and reduce the cost for the semiconductor package device, as shown by Rostoker et al.

- Regarding claim 50, Tanioka discloses the bare chip 7 is bonded to the substrate by wire bonding.
- Regarding claim 51, Tanioka discloses at least one chip package is a chip scale package or a wafer level chip scale package.
- Regarding claim 52, Tanioka discloses at least one chip package is chip scale package with wire bonding.
- Regarding claims 53-54, it would have been obvious to one having ordinary skill in the art to form one of the chip packages is a chip scale package with flip chip bonding or central pad bonding.
- Regarding claim 56, Tanioka discloses the plurality of electrical connect pins are solder balls 14.
- Regarding claim 57, Tanioka discloses the plurality of electrical connect points are wires.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN  
June 25, 2003

*Wael Fahmy*  
SPE 2814